Search History

STN
(Inspec, Heaphus, Japio, Wpadoc, uspatfull)
3/30/05

=> d l9 1-11 abs,bib

L9 ANSWER 1 OF 11 USPATFULL on STN
AB Disclosed herein is a method for forming a **silicon epitaxial layer**. The method comprises the steps of **cleaning** the **surface** of a silicon **substrate** having **dopant** of predetermined concentration doped therein with mixed plasma comprising an **etching gas** containing **fluorine** and hydrogen or **deuterium**, and forming a **silicon epitaxial layer** on the **cleaned surface** of the **silicon substrate**. The doped concentration of the silicon substrate is preferably 10.sup.18 to 10.sup.21 atoms/cm.sup.3. According to the present invention, a new preliminary cleaning step is adopted, whereby a **silicon epitaxial layer** of good quality is formed on a highly doped silicon substrate at a low temperature of 700° C. or less.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:158807 USPATFULL
TI Method for forming **silicon epitaxial layer**
IN Lee, Tae Wan, Seoul, KOREA, REPUBLIC OF
Choi, Kyu Jin, Kyunggi-do, KOREA, REPUBLIC OF
Sun, Jung Hoon, Kyunggi-do, KOREA, REPUBLIC OF
Whoang, Sung Jin, Kyunggi-do, KOREA, REPUBLIC OF
Cho, Bok Won, Kyunggi-do, KOREA, REPUBLIC OF
PA JUSUNG ENGINEERING CO., LTD., KWANGJU-GUN, KOREA, REPUBLIC OF (non-U.S. corporation)
PI US 2004121609 A1 20040624
AI US 2003-724187 A1 20031201 (10)
PRAI KR 2002-75765 20021202
DT Utility
FS APPLICATION
LREP OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VA, 22320
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 2 Drawing Page(s)
LN.CNT 209
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 2 OF 11 USPATFULL on STN
AB Raised structures comprising overlying **silicon layers** formed by controlled **selective epitaxial growth**, and methods for forming such raised-structure on a semiconductor substrate are provided. The structures are formed by selectively growing an initial **epitaxial layer** of monocrystalline **silicon** on the surface of a semiconductive substrate, and forming a thin film of insulative material over the epitaxial layer. A portion of the insulative layer is removed to expose the top surface of the epitaxial layer, with the insulative material remaining along the sidewalls as spacers to prevent lateral growth. A second epitaxial layer is selectively grown on the exposed surface of the initial epitaxially grown crystal layer, and a thin insulative film is deposited over the second epitaxial layer. Additional epitaxial layers are added as desired to provide a vertical structure of a desired height comprising multiple layers of single **silicon crystals**, each **epitaxial layer** have insulated sidewalls, with the uppermost epitaxial layer also with an insulated top surface. The resultant structure can function, for example, as a vertical gate of a DRAM cell, elevated source/drain structures, or other semiconductor device feature.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:236357 USPATFULL
TI Method for forming raised structures by controlled **selective epitaxial growth** of facet using spacer
IN Ping, Er-Xuan, Meridian, ID, UNITED STATES
McKee, Jeffrey A., Meridian, ID, UNITED STATES
PA Micron Technology, Inc., Boise, ID (U.S. corporation)
PI US 2003164513 A1 20030904
AI US 2003-379494 A1 20030304 (10)
RLI Division of Ser. No. US 2001-46497, filed on 26 Oct 2001, PENDING
Division of Ser. No. US 2001-816962, filed on 23 Mar 2001, PENDING
DT Utility
FS APPLICATION
LREP WHYTE HIRSCHBOECK DUDEK S.C., 111 E. WISCONSIN AVE., SUITE 2100, MILWAUKEE, WI, 53202
CLMN Number of Claims: 122
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 1043
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 3 OF 11 USPATFULL on STN
AB A method of manufacturing a semiconductor device comprising a plurality of single-crystal semiconductor layers formed, for example, in an opening of an insulating film, said semiconductor layers having no or very few crystal defects. The method comprises forming in a first growth chamber a first semiconductor layer of a first conductivity type in an opening of an insulating film and subsequently forming in a second growth chamber a second semiconductor layer of a second conductivity type in an opening of an insulating film, while supplying hydrogen to the surface of the substrate when the substrate is transferred from said first growth chamber to said second growth chamber.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:64941 USPATFULL
TI Semiconductor device and method for manufacturing the same
IN Oda, Katsuya, Hachioji, JAPAN
PA Hitachi, Ltd. (non-U.S. corporation)
PI US 2003045063 A1 20030306
AI US 2002-150943 A1 20020521 (10)
PRAI JP 2001-265362 20010903
DT Utility
FS APPLICATION
LREP Stanley P. Fisher, Reed Smith LLP, Suite 1400, 3110 Fairview Park Drive, Falls Church, VA, 22042-4503
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 26 Drawing Page(s)
LN.CNT 1721
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 4 OF 11 USPATFULL on STN
AB Raised structures comprising overlying **silicon layers** formed by controlled **selective epitaxial growth**, and methods for forming such raised-structure on a semiconductor substrate are provided. The structures are formed by selectively growing an initial **epitaxial layer** of monocrystalline **silicon** on the surface of a semiconductive substrate, and forming a thin film of insulative material over the epitaxial layer. A portion of the insulative layer is removed to expose the top surface of the epitaxial layer, with the insulative material remaining along the sidewalls as spacers to prevent lateral growth. A second epitaxial layer is selectively grown on the exposed surface of

the initial epitaxially grown crystal layer, and a thin insulative film is deposited over the second epitaxial layer. Additional epitaxial layers are added as desired to provide a vertical structure of a desired height comprising multiple layers of single **silicon crystals**, each **epitaxial layer** have insulated sidewalls, with the uppermost epitaxial layer also with an insulated top surface. The resultant structure can function, for example, as a vertical gate of a DRAM cell, elevated source/drain structures, or other semiconductor device feature.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:251321 USPATFULL
TI Method for forming raised structures by controlled **selective epitaxial growth** of facet using spacer
IN Ping, Er-Xuan, Meridian, ID, UNITED STATES
McKee, Jeffrey A., Meridian, ID, UNITED STATES
PI US 2002137269 A1 20020926
AI US 2001-46497 A1 20011026 (10)
RLI Division of Ser. No. US 2001-816962, filed on 23 Mar 2001, PENDING
DT Utility
FS APPLICATION
LREP WHYTE HIRSCHBOECK DUDEK S C, 111 EAST WISCONSIN AVENUE, SUITE 2100, MILWAUKEE, WI, 53202
CLMN Number of Claims: 122
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 1042
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 5 OF 11 USPATFULL on STN
AB Raised structures comprising overlying **silicon layers** formed by controlled **selective epitaxial growth**, and methods for forming such raised-structure on a semiconductor substrate are provided. The structures are formed by selectively growing an initial **epitaxial layer** of monocrystalline **silicon** on the surface of a semiconductive substrate, and forming a thin film of insulative material over the epitaxial layer. A portion of the insulative layer is removed to expose the top surface of the epitaxial layer, with the insulative material remaining along the sidewalls as spacers to prevent lateral growth. A second epitaxial layer is selectively grown on the exposed surface of the initial epitaxially grown crystal layer, and a thin insulative film is deposited over the second epitaxial layer. Additional epitaxial layers are added as desired to provide a vertical structure of a desired height comprising multiple layers of single **silicon crystals**, each **epitaxial layer** have insulated sidewalls, with the uppermost epitaxial layer also with an insulated top surface. The resultant structure can function, for example, as a vertical gate of a DRAM cell, elevated source/drain structures, or other semiconductor device feature.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:249115 USPATFULL
TI Method for forming raised structures by controlled **selective epitaxial growth** of facet using spacer
IN Ping, Er-Xuan, Meridian, ID, UNITED STATES
McKee, Jeffrey A., Meridian, ID, UNITED STATES
PI US 2002135029 A1 20020926
AI US 2001-816962 A1 20010323 (9)
DT Utility
FS APPLICATION
LREP WHYTE HIRSCHBOECK DUDEK S.C., 111 E. WISCONSIN AVE., SUITE 2100, MILWAUKEE, WI, 53202

CLMN Number of Claims: 122
ECL Exemplary Claim: 1
DRWN 7 Drawing Page(s)
LN.CNT 1042
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 6 OF 11 USPATFULL on STN
AB A method of manufacturing a semiconductor device including the steps of forming an insulating film on a silicon region of a substrate having the silicon region on a surface the insulating film having an opening for forming an exposed region of the silicon region, supplying a gas containing a halogen onto the silicon region, and supplying a source gas of silicon onto the silicon region, thereby selectively depositing the silicon on the exposed region of the silicon region.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:19244 USPATFULL
TI Semiconductor device and manufacturing method thereof
IN Mitani, Yuichiro, Yokohama, JAPAN
Mizushima, Ichiro, Yokohama, JAPAN
Kambayashi, Shigeru, Kawasaki, JAPAN
Nishino, Hirotaka, Pittsburgh, PA, United States
Kashiwagi; Masahiro, Yokohama, JAPAN
PA Kabushiki Kaisha Toshiba, Kawasaki, JAPAN (non-U.S. corporation)
PI US 6342421 B1 20020129
AI US 1998-98736 19980618 (9)
RLI Division of Ser. No. US 1995-526696, filed on 11 Sep 1995, now patented, Pat. No. US 5864161
PRAI JP 1994-218502 19940913
JP 1994-233934 19940929
JP 1995-84501 19950317
DT Utility
FS GRANTED
EXNAM Primary Examiner: Pham, Long; Assistant Examiner: Hawranek, Scott J
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN Number of Claims: 16
ECL Exemplary Claim: 1
DRWN 129 Drawing Figure(s); 33 Drawing Page(s)
LN.CNT 2651
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 7 OF 11 USPATFULL on STN
AB A manufacturing method produces a semiconductor IC device which can maintain a low power consumption for electronic circuits and form gate-isolation layers of different thicknesses without increasing the manufacturing cost. The semiconductor IC device has gate-isolation layers of different thicknesses on the same semiconductor substrate surface. To form such gate-isolation layers, a silicon dioxide layer is formed in first and second regions. The **dopant**-concentration is adjusted in silicon dioxide layer that is to have a thickness different from the above silicon dioxide layer thickness in the second region B. A carbon-containing semiconductor layer is selectively formed in either the first region or the second region. Therefore, there is no need for additional steps for forming silicon dioxide layers of different thicknesses in the first region and in the second region. In addition, a carbon-containing semiconductor layer is selectively formed on desired areas of the semiconductor substrate where thinner oxide layer is to be formed. The semiconductor substrate is oxidized successively to have oxide layers of different thickness on the surface of the substrate in one step.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:169951 USPATFULL

TI Semiconductor integrated circuit manufacturing method and device
IN Tsuchiaki, Masakatsu, Tokyo, Japan
PA TOSHIBA CORPORATION` (non-U.S. corporation)
PI US 2001025998 A1 20011004
US 6545327 B2 20030408
AI US 2001-845997 A1 20010430 (9)
RLI Division of Ser. No. US 1999-440958, filed on 16 Nov 1999, GRANTED, Pat. No. US 6271566
PRAI JP 1997-70998 19970325
JP 1997-217212 19970812
DT Utility
FS APPLICATION
LREP ANDERSON KILL & OLICK, P.C., 1251 Avenue of the Americas, New York, NY, 10020
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 15 Drawing Page(s)
LN.CNT 1439
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 8 OF 11 USPATFULL on STN
AB A manufacturing method produces a semiconductor IC device which can maintain a low power consumption for electronic circuits and form gate-isolation layers of different thicknesses without increasing the manufacturing cost. The semiconductor IC device has gate-isolation layers of different thicknesses on the same semiconductor substrate surface. To form such gate-isolation layers, a silicon dioxide layer is formed in first and second regions. The **dopant**-concentration is adjusted in silicon dioxide layer that is to have a thickness different from the above silicon dioxide layer thickness in the second region B. A carbon-containing semiconductor layer is selectively formed in either the first region or the second region. Therefore, there is no need for additional steps for forming silicon dioxide layers of different thicknesses in the first region and in the second region. In addition, a carbon-containing semiconductor layer is selectively formed on desired areas of the semiconductor substrate where thinner oxide layer is to be formed. The semiconductor substrate is oxidized successively to have oxide layers of different thickness on the surface of the substrate in one step.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:126319 USPATFULL
TI Semiconductor device having a carbon containing insulation layer formed under the source/drain
IN Tsuchiaki, Masakatsu, Tokyo, Japan
PA Toshiba Corporation, Tokyo, Japan (non-U.S. corporation)
PI US 6271566 B1 20010807
AI US 1999-440958 19991116 (9)
RLI Division of Ser. No. US 1998-47593, filed on 25 Mar 1998, now patented, Pat. No. US 6051509
PRAI JP 1997-70998 19970325
JP 1997-217212 19970812
DT Utility
FS GRANTED
EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Pham, Hoai
LREP Anderson, Kill & Olick P.C.
CLMN Number of Claims: 6
ECL Exemplary Claim: 1
DRWN 30 Drawing Figure(s); 15 Drawing Page(s)
LN.CNT 1315
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 9 OF 11 USPATFULL on STN

AB A manufacturing method produces a semiconductor IC device which can maintain a low power consumption for electronic circuits and form gate-isolation layers of different thicknesses without increasing the manufacturing cost. The semiconductor IC device has gate-isolation layers of different thicknesses on the same semiconductor substrate surface. To form such gate-isolation layers, a silicon dioxide layer is formed in first and second regions. The **dopant**-concentration is adjusted in silicon dioxide layer that is to have a thickness different from the above silicon dioxide layer thickness in the second region B. A carbon-containing semiconductor layer is selectively formed in either the first region or the second region. Therefore, there is no need for additional steps for forming silicon dioxide layers of different thicknesses in the first region and in the second region. In addition, a carbon-containing semiconductor layer is selectively formed on desired areas of the semiconductor substrate where thinner oxide layer is to be formed. The semiconductor substrate is oxidized successively to have oxide layers of different thickness on the surface of the substrate in one step.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2000:47166 USPATFULL
TI Semiconductor integrated circuit manufacturing method and device
IN Tsuchiaki, Masakatsu, Tokyo, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 6051509 20000418
AI US 1998-47593 19980325 (9)
PRAI JP 1997-70998 19970325
JP 1997-217212 19970812
DT Utility
FS Granted
EXNAM Primary Examiner: Niebling, John F.; Assistant Examiner: Jones, Josetta
LREP Meller, Michael N., Lieberstein, Eugene
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 30 Drawing Figure(s); 15 Drawing Page(s)
LN.CNT 1384
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 10 OF 11 USPATFULL on STN
AB A method of manufacturing a semiconductor device includes the steps of forming an insulating film on a silicon region of a substrate having the silicon region on a surface the insulating film having an opening for forming an exposed region of the silicon region, supplying a gas containing a halogen onto the silicon region, and supplying a source gas of silicon onto the silicon region, thereby selectively depositing the silicon on the exposed region of the silicon region.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 1999:13167 USPATFULL
TI Semiconductor device and manufacturing method thereof
IN Mitani, Yuichiro, Yokohama, Japan
Mizushima, Ichiro, Yokohama, Japan
Kambayashi, Shigeru, Kawasaki, Japan
Nishino, Hirotaka, Pittsburgh, PA, United States
Kashiwagi, Masahiro, Yokohama, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 5864161 19990126
AI US 1995-526696 19950911 (8)
PRAI JP 1994-218502 19940913
JP 1994-233934 19940929
JP 1995-84501 19950317
DT Utility
FS Granted

EXNAM Primary Examiner: Fahmy, Wael
LREP   Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN   Number of Claims: 5
ECL   Exemplary Claim: 1
DRWN   129 Drawing Figure(s); 33 Drawing Page(s)
LN.CNT 2568
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9   ANSWER 11 OF 11 USPAT2 on STN
AB   A manufacturing method produces a semiconductor IC device which can maintain a low power consumption for electronic circuits and form gate-isolation layers of different thicknesses without increasing the manufacturing cost. The semiconductor IC device has gate-isolation layers of different thicknesses on the same semiconductor substrate surface. To form such gate-isolation layers, a silicon dioxide layer is formed in first and second regions. The **dopant**-concentration is adjusted in silicon dioxide layer that is to have a thickness different from the above silicon dioxide layer thickness in the second region B. A carbon-containing semiconductor layer is selectively formed in either the first region or the second region. Therefore, there is no need for additional steps for forming silicon dioxide layers of different thicknesses in the first region and in the second region. In addition, a carbon-containing semiconductor layer is selectively formed on desired areas of the semiconductor substrate where thinner oxide layer is to be formed. The semiconductor substrate is oxidized successively to have oxide layers of different thickness on the surface of the substrate in one step.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN   2001:169951 USPAT2
TI   Semiconductor device having different gate insulating films with different amount of carbon
IN   Tsuchiaki, Masakatsu, Tokyo, JAPAN
PA   Toshiba Corporation, Tokyo, JAPAN (non-U.S. corporation)
PI   US 6545327   B2   20030408
AI   US 2001-845997   20010430 (9)
RLI   Division of Ser. No. US 1999-440958, filed on 16 Nov 1999, now patented, Pat. No. US 6271566 Division of Ser. No. US 1998-47593, filed on 25 Mar 1998, now patented, Pat. No. US 6051509
PRAI   JP 1997-70998   19970325
       JP 1997-217212   19970812
DT   Utility
FS   GRANTED
EXNAM Primary Examiner: Fahmy, Wael; Assistant Examiner: Pham, Hoai
LREP   Anderson Kill & Olick, Lieberstein, Eugene, Meller, Michael N.
CLMN   Number of Claims: 10
ECL   Exemplary Claim: 1
DRWN   30 Drawing Figure(s); 15 Drawing Page(s)
LN.CNT 1336
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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     (FILE 'HOME' ENTERED AT 12:14:53 ON 30 MAR 2005)

     FILE 'STNGUIDE' ENTERED AT 12:14:58 ON 30 MAR 2005

     FILE 'HCAPLUS, INPADOC, JAPIO, USPATFULL, USPAT2' ENTERED AT 12:15:39 ON 30 MAR 2005

     FILE 'HCAPLUS, INPADOC, USPATFULL, USPAT2, JAPIO, INSPEC' ENTERED AT 12:15:54 ON 30 MAR 2005

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L1        246228 S (SI OR SILICON)(8A)(EPITAX?(4A)LAYER# OR EPITAX? OR CRYSTAL?)
L2         14253 S (CLEAN?)(8A)(SURFACE(6A)SUBSTRATE)
L3        178210 S (DOPANT#)
L4         52322 S (ETCH?(6A)GAS?)
L5          7935 S (SEG OR SELECTIVE(W)EPITAXIAL(W)GROWTH)
L6        666012 S (FLUORINE OR H2 OR HYDROGEN RO D2 OR DEUTERIUM)
L7            63 S L1 AND L2 AND L3 AND L4 AND L6
L8           551 S L5 AND L6
L9            11 S L5 AND L7

=>
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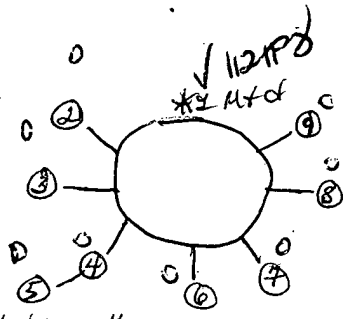
09/724,187 Examiner's Notes

S(Si or silicon)(10a)(epitaxy)(4a) layer or epitaxial or crystal?)
S(clean?)(10a)(surface(6a) substrate)
S(dopant#)
S(plasma)
S(etch?(6a) gas?)
S(For flourine or H_2 or hydrogen or deuterium or D_2)
S(SEG or selective(w)epitaxial(w)growth)



112P2 Rej
Claim 1, line 6 "predetermined concentration..."
Claim 1, line 6 "...dopant... (No antecedence)

Day : Wednesday

PALM INTRANET

Date: 3/30/2005
Time: 12:11:59

Inventor Name Search Result

Your Search was:

Last Name = LEE
First Name = TAE WAN

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** Lee **First Name** Tae Wan Search

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Day : Wednesday

PALM INTRANET

Date: 3/30/2005
Time: 12:12:16

Inventor Name Search Result

Your Search was:

Last Name = CHOI
First Name = KYU JIN

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** Choi **First Name** Kyu Jin Search

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Day : Wednesday

PALM INTRANET

Date: 3/30/2005
Time: 12:12:36

Inventor Name Search Result

Your Search was:

Last Name = SUN
First Name = JUNG HOON

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** Sun **First Name** Jung Hoon Search

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Day : Wednesday

PALM INTRANET

Date: 3/30/2005
Time: 12:12:52

Inventor Name Search Result

Your Search was:

Last Name = CHO
First Name = BOK WON

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09469257	6566221	150	12/22/1999	CAPACITOR STRUCTURE AND METHOD FOR FABRICATING THE SAME	CHO, BOK WON

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** Cho **First Name** Bok Won Search

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